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| 10/663,485 | 09/15/2003 | Takashi Kumamoto | 109263-131564 | 2427 |

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| EXAMINER | |
|---|---|
| VU, QUANG D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/663,485 | KUMAMOTO, TAKASHI | |
| | Examiner | Art Unit | |
| | Quang D. Vu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7-15 and 17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15 and 17-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

The finality of the rejection of the last Office action is withdrawn in view of the present Office action.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 7, 8, 9, 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 6,507,102 to Juskey et al.

For this rejection, note the attached marked up copy of figure 2 of Isaak.

Regarding claim 1, Isaak (figures 1-8) teaches a microelectronic package array, comprising:

a first microelectronic package (12b) including a first carrier substrate (14b) having a first die side (16b) and a first non-die side (18b), a first die (70b) electrically coupled to the first die side (16b), and a land pad (pad [26b]) on the first die side (16b);

a second microelectronic package (12a) comprising a second carrier substrate (14a) having a second die side (16a) and a second non-die side (18a), a second die (70a) electrically

coupled to the second die side (16a), and a bond pad (pad [30a]) on the second non-die side (18a); and

an intermediate substrate (34) having a first side (a top surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]), the first side (a top surface of the substrate [34]) being coupled to the first die side (16b) of the first carrier substrate (14b) and the second side (a bottom surface of the substrate [34]) being coupled to the second non-die side (18a) of the second carrier substrate (14a), the intermediate substrate (34) comprising of a substantially solid core having a first side (a top surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]).

Isaak differs from the claimed invention by not showing the substrate comprising a material reinforced with a matrix. However, Juskey et al. teach an epoxy resin to form a matrix (column 3, line 66 - column 4, line 9). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Juskey et al. into the device taught by Isaak in order to provide an excellent mechanical and thermal properties of the material.

Note that a material reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Isaak and Juskey et al. could have been used for the claimed purpose.

Regarding claim 2, the combined device shows an adhesive material (Isaak; a portion of the layer [49]) disposed on the first side (Isaak; top surface of the substrate [34]) and second side

(Isaak; bottom surface of the substrate [34]) of the core; and a conductive riser (Isaak; 32) disposed within the solid core (Isaak; a portion of the intermediate substrate [34]).

Regarding claim 3, the combined device shows the intermediate substrate (Isaak; 34) is mechanically bonded to the first die side (Isaak; 16b) of the first carrier substrate (Isaak; 14b) and the second non-die side (Isaak; 18a) of the second carrier substrate (Isaak; 14a) by the adhesive material (Isaak; a portion of the layer [49]).

Regarding claim 5, the combined device shows the material is a C-stage resin (Juskey et al.; column 3, line 66 - column 4, line 9).

Regarding claim 7, the combined device shows the substrate (Juskey et al.; 14) is selected from fiberglass.

Regarding claim 8, the combined device shows the conductive riser (Isaak; 32) is electrically coupled to the land pad (Isaak; 26b) of the first microelectronic package (Isaak; 12b) and the bond pad (Isaak; 30a) of the second microelectronic package (Isaak; 12a).

Regarding claim 9, the combined device shows the conductive riser (Isaak; 32) includes a first end (Isaak; an upper portion of [32]) and a second end (Isaak; a lower portion of [32]) having conductive plating (Isaak; a portion of [51]) disposed thereon, the first (Isaak; an upper portion of [32]) and second (Isaak; a lower portion of [32]) ends being electrically bonded to the land pad (Isaak; 26b) and the bond pad (Isaak; 30a) respectively by the conductive plating (Isaak; a portion of [51]).

Regarding claim 21, Isaak (figures 1-8) teaches a method for fabricating a microelectronic package array, comprising:

providing a first microelectronic package (12b) having a first carrier substrate (14b) with a first die side (16b) and a first non-die side (18b), and a plurality of land pads (pads [26b]) disposed on the first die side (16b);

a second microelectronic package (12a) comprising a second carrier substrate (14a) with a second die side (16a) and a second non-die side (18a), and a plurality of bond pad (pads [30a]) disposed on the second non-die side (18a); and

placing an intermediate substrate (34) having a plurality of conductive risers (32) disposed therein on the first die side (16b) of a the first carrier substrate (14b), the intermediate substrate (34) comprising of a substantially solid core having a first side (a top surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]);

placing the second carrier substrate (14a) on the intermediate substrate (34) with the second non-die side (18a) coming in contact with the intermediate substrate (34);

mechanically coupling the intermediate substrate (34) to the first (14b) and second (14a) carrier substrates; and

electrically coupling the plurality of conductive risers (32) with the plurality of land (26b) and bond pads (30a).

Isaak differs from the claimed invention by not showing the substrate comprising a material reinforced with a matrix. However, Juskey et al. teach an epoxy resin to form a matrix (column 3, line 66 - column 4, line 9). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Juskey et al. into the device taught by Isaak in order to provide an excellent mechanical and thermal

properties of the material. The combined device shows a material reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate.

Regarding claim 26, the combined device shows an adhesive material (Isaak; a portion of layer 49) disposed on the first side (Isaak; top surface of the substrate [34]) and the second side (Isaak; bottom surface of the substrate [34]).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Juskey et al., and further in view of US Patent No. 6,014,317 to Sylvester.

Regarding claim 4, the disclosures of Isaak and Juskey et al. are discussed as applied to claims 1-3, 5, 7, 8 and 9 above.

The combined device differs from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Sylvester teaches the B-stage adhesive material (column 21, lines 23-28). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sylvester into the device taught by Isaak and Juskey et al. in order to improve the molding characteristics of the adhesive material.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Juskey et al., and further in view of US Patent Applicant Publication No. 2004/0050586 to Roh.

Regarding claim 10, the disclosures of Isaak and Juskey et al. are discussed as applied to claims 1-3, 5, 7, 8 and 9 above.

The combined device differs from the claimed invention by not showing the conductive plating is tin. However, Roh teaches the conductive plating is tin (paragraph [0033]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Roh into the device taught by Isaak and Juskey et al. in order to improve the conductivity of the device.

5. Claims 11-13, 15, 17, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 6,054,337 to Solberg and US Patent No. 6,507,102 to Juskey et al.

Regarding claim 11, Isaak (figures 1-8) teaches a system, comprising:

a system board (printed circuit board; paragraph [0052]);

a memory (memory chip; paragraph [0003]) configured to store data, the memory disposed on the system board;

a microelectronic package array (10) disposed on the system board (printed circuit board; paragraph [0052]), the microelectronic package array comprising:

a first microelectronic package (12b) including a first carrier substrate (14b) having a first die side (16b) and a first non-die side (18b), a first die (70b) electrically coupled to the first die side (16b), and a land pad (pad [26b]) on the first die side (16b);

a second microelectronic package (12a) comprising a second carrier substrate (14a) having a second die side (16a) and a second non-die side (18a), a second die (70a) electrically coupled to the second die side (16a), and a bond pad (pad [30a]) on the second non-die side (18a); and

an intermediate substrate (34) coupled to the first die side (16b) of the first carrier substrate (14b) and the second non-die side (18a) of the second carrier substrate (14a), the intermediate substrate (34) comprising of a substantially solid core having a first side (a top surface of the substrate [34]) and a second (a bottom surface of the substrate [34]) side.

Isaak differs from the claimed invention by not showing the memory coupled to the bus. However, Solberg teaches the memory chips, which are connected to the data bus (column 2, lines 55-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Solberg into the device taught by Isaak in order to provide interconnect between the chip and the external device. The combined device shows a bus disposed on the system board to facilitate data exchange; a memory configured to store data, the memory disposed on the system board and coupled to the bus; and a microelectronic package array disposed on the system board and coupled to the bus.

The combined device differs from the claimed invention by not showing the substrate comprising a material reinforced with a matrix. However, Juskey et al. teach an epoxy resin to form a matrix (column 3, line 66 - column 4, line 9). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Juskey et al. into the device taught by Isaak and Solberg in order to provide an excellent mechanical and thermal properties of the material.

Note that a material reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate is a function al language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Isaak, Solberg and Juskey et al. could have been used for the claimed purpose.

Regarding claim 12, the combined device shows an adhesive material (Isaak; a portion of the layer [49]) disposed on the first side (Isaak; top surface of the substrate [34]) and second side (Isaak; bottom surface of the substrate [34]) of the core; and a conductive riser (Isaak; 32) disposed within the solid core (Isaak; a portion of the intermediate substrate [34]).

Regarding claim 13, the combined device shows the intermediate substrate (Isaak; 34) is mechanically bonded to the first die side (Isaak; 16b) of the first carrier substrate (Isaak; 14b) and the second non-die side (Isaak; 18a) of the second carrier substrate (Isaak; 14a) by the adhesive material (Isaak; a portion of the layer [49]).

Regarding claim 15, the combined device shows the material is a C-stage resin (Juskey et al.; column 3, line 66 - column 4, line 9).

Regarding claim 17, the combined device shows the substrate (Juskey et al.; 14) is selected from fiberglass.

Regarding claim 18, the combined device shows the conductive riser (Isaak; 32) is electrically coupled to the land pad (Isaak; 26b) of the first microelectronic package (Isaak; 12b) and the bond pad (Isaak; 30a) of the second microelectronic package (Isaak; 12a).

Regarding claim 19, the combined device shows the conductive riser (Isaak; 32) includes a first end (Isaak; an upper portion of [32]) and a second end (Isaak; a lower portion of [32]) having conductive plating (Isaak; a portion of [51]) disposed thereon, the first (Isaak; an upper portion of [32]) and second (Isaak; a lower portion of [32]) ends being electrically bonded to the land pad (Isaak; 26b) and the bond pad (Isaak; 30a) respectively by the conductive plating (Isaak; a portion of [51]).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak and Solberg in view of Juskey et al., and further in view of US Patent No. 6,014,317 to Sylvester.

Regarding claim 14, the disclosures of Isaak, Solberg and Jeskey et al. are discussed as applied to claims 11-13, 15, 17 18 and 19 above.

The combined device differs from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Sylvester teaches the B-stage adhesive material (column 21, lines 23-28). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sylvester into the device taught by Isaak, Solberg and Juskey et al. in order to improve the molding characteristics of the adhesive material.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak and Solberg in view of Juskey et al., and further in view of US Patent Applicant Publication No. 2004/0050586 to Roh.

Regarding claim 20, the disclosure of Isaak, Solberg and Juskey et al. are discussed as applied to claims 11-13, 15, 17, 18 and 19 above.

The combined device differs from the claimed invention by not showing the conductive plating is tin. However, Roh teaches the conductive plating is tin (paragraph [0033]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Roh into the device taught by Isaak, Solberg and Juskey et al. in order to improve the conductivity of the device.

8. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Juskey et al., and further in view of US Patent No. 5,145,303 to Clarke.

Regarding claim 22, the disclosures of Isaak and Juskey et al. are discussed as applied to claims 21 and 26 above.

The combined device differs from the claimed invention by not showing placing the microelectronic package array in a vacuum chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array. However, Clarke teaches the microelectronic package in processing chamber (column 1, lines 15-19). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Clarke into the device taught by Isaak and Juskey et al. in order to enhance the performance and to improve reliability of the microelectronic package. The combined device shows placing the microelectronic package array in a vacuum chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array.

Regarding claim 23, the combined device differs from the claimed invention by not showing creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals in order to enhance the performance and to improve reliability of the microelectronic package.

Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 24, the combined device differs from the claimed invention by not showing applying heat comprises raising the temperature to about between $150^0$C and $350^0$C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying heat comprises raising the temperature to about between $150^0$C and $350^0$C in order to enhance the performance and to improve reliability of the microelectronic package. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 25, the combined device differs from the claimed invention by not showing applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals in order to enhance the performance and to improve reliability of the microelectronic package. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Juskey et al., and further in view of US Patent No. 6,014,317 to Sylvester.

Regarding claim 27, the disclosures of Isaak and Juskey et al. are discussed as applied to claims 21 and 26 above.

The combined device shows the material is a C-stage resin (Juskey et al.; column 3, line 66 - column 4, line 9).

The combined device differs from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Sylvester teaches the B-stage adhesive material (column 21, lines 23-28). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sylvester into the device taught by Isaak and Juskey et al. in order to improve the molding characteristics of the adhesive material.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-5, 7-15 and 17-27 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
April 14, 2005

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